IN THE SPECIFICATION:

Please amend the following paragraph [0044] in the present published application US 2005/0278588 as follows:

[0044] Based upon bit mapping 41 of the scan chain data, as the scan chain bits pass through the input fix register, a hold latch is provided to capture an incoming bit stream. If the program count is a match, an output latch captures the correct logic EC scan bit(s).

Please amend the following paragraph [0046] in the present published application US 2005/0278588 as follows:

[0046] Breakpoints can be set by any one of several possible approaches, such as by a comparison with the program count of the program counter, indicated schematically at 42, or by another architecture compare function that the designer implements as part of the design process. Another approach could be based upon the number of clock cycles, with a number of clock cycles being selected to provide a given multiplication effect. Once a breakpoint is reached, the EC function triggers a halt of the system clock, by issuing a clock halt signal 44, and then the scan chains and FPGA macros execute to provide the EC logic function.